Amin Mamandipoor

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EXPERIENCES

University of Kansas **January 2024 – Present**
Graduate Teaching Assistant *Lawrence, KS*

- **Introduction to Computer Architecture** (EECS645)
- Held weekly office hours to answer students' questions

University of Kansas **January 2022 – December 2023**
Graduate Research Assistant *Lawrence, KS*

- Analyzed the performance of heterogeneous multi-accelerators in datacenters
- Profiled gem5 for designing a specialized core for running architectural simulations
- RTL design of network protocols accelerator on AxDIMM
- Enhanced gem5's memory subsystem for intelligent cleaning of dirty cachelines

University of Tabriz **Sep 2017 – May 2020**
Graduate Teaching Assistant *Tabriz, Iran*

- ***Introduction to Computer Architecture*** and ***Digital Circuit Design***
- Graded homework and programming assignments

EDUCATION

University of Kansas, Lawrence **2022 - 2026 (*expected*)**
Ph.D. in Computer Science; GPA: 3.97/4
Advisor: Prof. Mohammad Alian

University of Tabriz, Iran **2018 - 2021**
M.Sc. in Computer Engineering

University of Tabriz, Iran **2013 - 2018**
B.Sc. in Computer Engineering

TECHNICAL SKILLS

Languages: C/C++, Python, Java, Verilog, MIPS assembly

Software & Tools: gem5, ModelSim, Cadence Virtuoso, Vivado HLS, Vitis AI, MATLAB, Git, Docker, Intel PIN, Intel Vtune, Intel CAT

AWARDS

First Place, I2S Student Research Symposium **2024**

Second Runner-up, Open Innovation Contest for AxDIMM Technology by Samsung **2022**

Outstanding Student Award, University of Tabriz **2014,2021**

Ranked 4th/20, FPGA Challenge Competition, AUT, Iran **2014**

PROJECTS

Operating Systems: Quash **Fall 2022**

Implemented the Quash command-line interface, akin to bash, featuring user input parsing, dynamic pipeline detection, tokenization with custom delimiters, and command execution in C.

VLSI Design: 8-bit Counter **Spring 2019**

Developed an 8-bit counter using Cadence Virtuoso, leveraging TSMC's 180nm process technology. Utilized schematic capture, layout design, and DRC/LVS validation to ensure optimal performance and reliability in VLSI circuits.

Genetic Algorithm for N-Queen Puzzle Optimization **Spring 2016**

Implemented in Java, leveraging computational intelligence techniques to navigate the vast solution space, ensuring rapid convergence through optimized selection, crossover, and mutation operations.

PUBLICATIONS

• Neel Patel, **Amin Mamandipoor**, Derrick Quinn, and Mohammad Alian, "XFM: Accelerated Software-Defined Far Memory," MICRO 2023

• Johnson Umeike, Neel Patel, Alex Manley, **Amin Mamandipoor**, Heechul Yun, Mohammad Alian, "Profiling gem5 Simulator," ISPASS 2023

• Neel Patel, **Amin Mamandipoor**, Mohammad Alian, "SmartDIMM: In-Memory Acceleration of Upper Layer I/O Protocols," HPCA 2024

• Shu-Ting Wang, Hanyang Xu, **Amin Mamandipoor**, Rohan Mahapatra, Byung Hoon Ahn, Soroush Ghodrati, Krishnan Kailas, Mohammad Alian, Hadi Esmaeilzadeh, "Data Motion Acceleration for Heterogeneous Cross Domain Accelerator Chaining," HPCA 2024

RESEARCH INTERESTS

Near-Memory Processing, Datacenter Networking, Computer Architecture, Memory Subsystem, I/O Subsystem, Domain Specific Accelerators, VLSI Design

TALKS

SmartDIMM: In-Memory Acceleration of Upper Layer I/O Protocols **November 2023**

SRC JUMP 2.0